A Fully Integrated CMOS RF Power Amplifier with Internal Frequency Doubling

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Presentation outline

• Introduction
• PA Analysis
• Implementation
• Results
• Conclusion
Motivation

• High level of integration
  ➔ on-chip impedance transformation network
  ➔ no discrete “RF choke” inductor

• Constant-envelope modulation
  ➔ non-linear PA

• VCO - PA disturbance
  ➔ frequency multiplication

• Medium output power
  ➔ class C
**Frequency Doubling PA**

- A narrowband FM input signal:
  \[ x(t) = A \cos \omega_c t - Am \sin (\omega_c t) \int x_{BB}(t) dt \]
  *where* \( m \int x_{BB}(t) dt \ll 1 \)

- 2nd order harmonic:
  \[ x^2(t) \approx A^2 \left[ DC + \frac{1}{2} \cos (2\omega_c t) - m \sin (2\omega_c t) \int x_{BB}(t) dt \right] \]

  ➞ same signal information as in fundamental
  ➞ double phase shift
**Frequency Doubling, Cont’d**

PA stage with cancelled odd harmonics:

Differential version:
**Ideal PA response**

- **DC current:**
  \[ I_{DC} = \frac{I_{max}}{2\pi} \cdot \frac{2\sin(\alpha/2) - \alpha \cos(\alpha/2)}{1 - \cos(\alpha/2)} \]

  \( I_{max} = \) maximum output current

  \( \alpha = \) conduction angle
**Ideal PA response**

- **DC current:**
  \[
  I_{DC} = \frac{I_{\text{max}}}{2\pi} \cdot \frac{2 \sin \alpha/2 - \alpha \cos \alpha/2}{1 - \cos \alpha/2}
  \]
  
  \(I_{\text{max}}\) = maximum output current  
  \(\alpha\) = conduction angle

- **2nd order harmonic:**
  \[
  I_2 = \frac{1}{\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{\text{max}}}{1 - \cos \alpha/2} \left[ \cos \theta - \cos \alpha/2 \right] \cos 2\theta \, d\theta = \frac{I_{\text{max}}}{2\pi} \cdot \frac{1}{1 - \cos \alpha/2} \left( -\frac{1}{3} \sin \frac{3\alpha}{2} + \sin \frac{\alpha}{2} \right)
  \]

⇒ **Drain efficiency for 2nd harmonic:**

\[
\eta_2 = \frac{P_2}{P_{\text{DC}}} = \frac{V_{DD}I_2}{2V_{DD}I_{DC}} = \frac{1}{2} \left( \frac{\sin \frac{\alpha}{2} - \frac{1}{3} \sin \frac{3\alpha}{2}}{2 \sin \alpha/2 - \alpha \cos \alpha/2} \right)
\]
**Ideal PA Response, Cont’d**

Output signals and efficiency vs. conduction angle:

\[ I_1, I_2, I_{dc} \]

\[ \eta_1, \eta_2 \]

(I_i = normalized)

Assumptions: no knee voltage, optimized load impedance, ideal transformation network, termination of irrelevant harmonics.
**Non-ideal efficiency**

- **Knee voltage**
  \[ \eta_{knee} = \frac{V_{DD} - V_{knee}}{V_{DD}} \]

- **Transformation network**
  with \( L_1 \) \( Q \) factor of 12:
  \[ \eta_Q = 75\%, \text{ or } -1.2\text{dB}. \]

**Combined efficiency example:**
- **With:** \( \alpha = 2.1, \frac{V_{knee}}{V_{DD}} = 0.1, Q_{L1} = 12: \)
  \[ \eta_{tot} = \eta_2 \eta_{knee} \eta_Q = 0.64 \times 0.9 \times 0.75 = 0.43 = 43\% \]
**Stand-alone power amplifier**

- Polyphase network to generate I/Q signals
PA with VCO

- Varactor with continuous and discrete tuning

\[ f_{\text{out}} = 2f_{\text{VCO}} \]
Chip micrograph

- PA + VCO

<table>
<thead>
<tr>
<th></th>
<th>stand-alone PA</th>
<th>PA + VCO</th>
</tr>
</thead>
<tbody>
<tr>
<td>active area</td>
<td>1.44 mm(^2)</td>
<td>2.25 mm(^2)</td>
</tr>
</tbody>
</table>
Results

Stand-alone PA

Output power

Drain efficiency

Stand-alone PA; VddDR=3.3

Stand-alone PA; Vdd,PA=3

Stand-alone PA; Vdd,PA=3.3
**Results**

**PA + VCO**

- Varying $V_{DD, VCO}$:

  **Output power**

  ![Output power graph](image)

  **Drain efficiency**

  ![Drain efficiency graph](image)
**Results**

**PA + VCO, Cont’d**

- **Varying \( V_{DD}, PA \):**
  - **Output power**
  - **Drain efficiency**

![Graphs showing output power and drain efficiency vs. supply voltage](image-url)
Results

PA + VCO, Cont’d

- Varying Vctrl:
  - Output frequency
  - Output power, drain efficiency

![Graph showing output frequency and power vs. Vctrl](image)

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PA + VCO, Cont’d

Frequency response of PA stage:

![Frequency response graph](image-url)

- ** fout [GHz] **
- ** Pout [dBm] **
- ** Vdd,PA=3.3 **
## Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>maximum PA output power</td>
<td>15 dBm</td>
</tr>
<tr>
<td>maximum PA drain efficiency</td>
<td>10.7%</td>
</tr>
<tr>
<td>VCO frequency range</td>
<td>1.522-1.637GHz</td>
</tr>
<tr>
<td>active area: stand-alone PA</td>
<td>1.44 mm(^2)</td>
</tr>
<tr>
<td>VCO + PA</td>
<td>2.25 mm(^2)</td>
</tr>
</tbody>
</table>
### Results

#### Comparison to other work

Fully integrated CMOS power amplifiers:

<table>
<thead>
<tr>
<th></th>
<th>Pout (dBm)</th>
<th>freq. (GHz)</th>
<th>efficiency (max)</th>
<th>technology</th>
<th>output matching</th>
<th>other</th>
<th>class</th>
</tr>
</thead>
<tbody>
<tr>
<td>[2]</td>
<td>33.4 (@max PAE)</td>
<td>2.4</td>
<td>31% (PAE)</td>
<td>0.35um (Bi)CMOS</td>
<td>on-chip</td>
<td>-</td>
<td>E/F3</td>
</tr>
<tr>
<td>[3]</td>
<td>20 (max)</td>
<td>1.9</td>
<td>16% (η)</td>
<td>0.8um CMOS</td>
<td>on-chip</td>
<td>-</td>
<td>F?</td>
</tr>
<tr>
<td>[4]</td>
<td>17.5 (max)</td>
<td>2.4</td>
<td>16.4% (PAE)</td>
<td>0.35um CMOS</td>
<td>partly on-chip</td>
<td>-</td>
<td>A</td>
</tr>
<tr>
<td>[5]</td>
<td>9 (@P-5dB)</td>
<td>2.4</td>
<td>16% (P-5dB)</td>
<td>0.18um CMOS</td>
<td>partly on-chip</td>
<td>-</td>
<td>AB?</td>
</tr>
<tr>
<td>[6]</td>
<td>18.6 (@max PAE)</td>
<td>0.9</td>
<td>30% (PAE max)</td>
<td>0.6um CMOS</td>
<td>on-chip</td>
<td>-</td>
<td>C</td>
</tr>
<tr>
<td>this work</td>
<td>15 (max)</td>
<td>2.4</td>
<td>10.7% (η)</td>
<td>0.18um CMOS</td>
<td>on-chip</td>
<td>freq. doubl.</td>
<td>C</td>
</tr>
</tbody>
</table>

Both the efficiency and the output power are degraded since the 2nd harmonic is taken instead of the fundamental!
**Conclusions**

Design and measurement of a CMOS class C PA:

- with internal frequency doubling
- fully integrated, including impedance transformation network
- with drain efficiency analysis
- 2 test chips: a stand-alone PA and PA with VCO
- max. drain efficiency = 10.7%
  max. output power = 15 dBm