A Digitally Controlled PLL using a Standard Cell Library

Thomas Olsson and Peter Nilsson

Dept. of Electroscience, Lund University.
Why use a PLL?

- Locally optimized clocks.
  - \( P = fC V_{dd}^2 \), possible savings.
- Higher clock frequency for higher throughput.
- Limit clock skew.
  - Remove delay from clock buffers.
All-Digital PLL clock multiplier

- Digital PLL used as a clock multiplier.
- Standard cell design, 0.35 μm CMOS.
- 150 MHz to 360 MHz @ 3.0 V supply.
- Core area 0.07 mm².
Block schedule

Block diagram:

- REF
- Ph-det
- EVENT
- *UPDATE
- T2d
- /M
- BUF
- clk_out
- DCO
- UP/DOWN
- +/-
- REG
- Recursive filter
- 0.5
- X
- 0.5
Phase detector

- Modified standard type
- Small offset error
Phase detector cont.

• 1.40 ns phase error
  ⇒ Simulated phase error measurement (EVENT) of 1.42 ns
DCO

- 7-stage ring oscillator
- Frequency control using parallel tri-state gates
- Only standard cells.
  - No layout tools required
  - Performance degradation compared to full custom
- 7 bit control word \( W \) \( \Rightarrow \) 126 bit \( C \) to guarantee monotonic behavior.
  \[ W=0000010 \Rightarrow C=00111111111111……. \]
DCO performance

- Measured frequency range: 150-360 MHz @ 3.0 V supply.
- Nonlinear but monotonic.
- Slope between 10 and 150 Ps/bit.
Step response

- About 20 iteration periods to lock.
- Oscillates between adjacent control words at phase lock.
Power consumption / lock range vs. supply voltage

- @ 3.0 V: 150 MHz – 360 MHz, 8.1 mW – 24 mW.
- @ 2.0 V: 90 MHz – 230 MHz, 2.1 mW – 6.1 mW.
- Lock range equal to DCO frequency range.
Improved design

• A synthesizable VHDL description of the PLL.
  ⇒ Simulate PLL in digital simulator to radically decrease simulation time.
  System simulation in digital simulator.
  Easy to change process.

• PLL control independent of oscillator frequency.
  ⇒ New time to digital converter is designed.

• Optimized digital filter to shorten lock time.

• Improved DCO using a D/A converter and a VCO.
  ⇒ Higher output frequency $\leq 1$ GHz.

• Analog design and simulation of DCO only.

• Sent for fabrication.
Time to digital converter

- Resolution ~ 250 ps.
DCO(2)

- Simulated frequency range: 210 – 910 MHz @ 3.0 V supply.
- Nonlinear but monotonic.
- Slope between 5 and 70 Ps/bit.
VHDL simulation of step response

- About 10 iteration periods to lock.
- Oscillates between adjacent control words at phase lock.
- Analog simulation data from DCO.
Summary

• A prototype of an all-digital PLL is designed using a 0.35 µm CMOS process.
  ⇨ Frequency range: 150 – 360 MHz @ 3.0 V.
  ⇨ Power consumption: 8.1 – 24 mW @ 3.0 V.
  ⇨ Implemented using cells found in an ordinary standard-cell library.
  ⇨ Core area 0.07 mm².

• Next version is implemented in synthesizable VHDL-code except for the DCO.
  ⇨ Frequency range of 210-910 MHz.
  ⇨ Time-to digital converter with ~ 250 ps resolution.